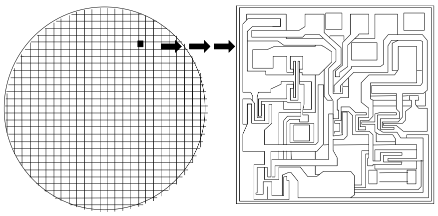
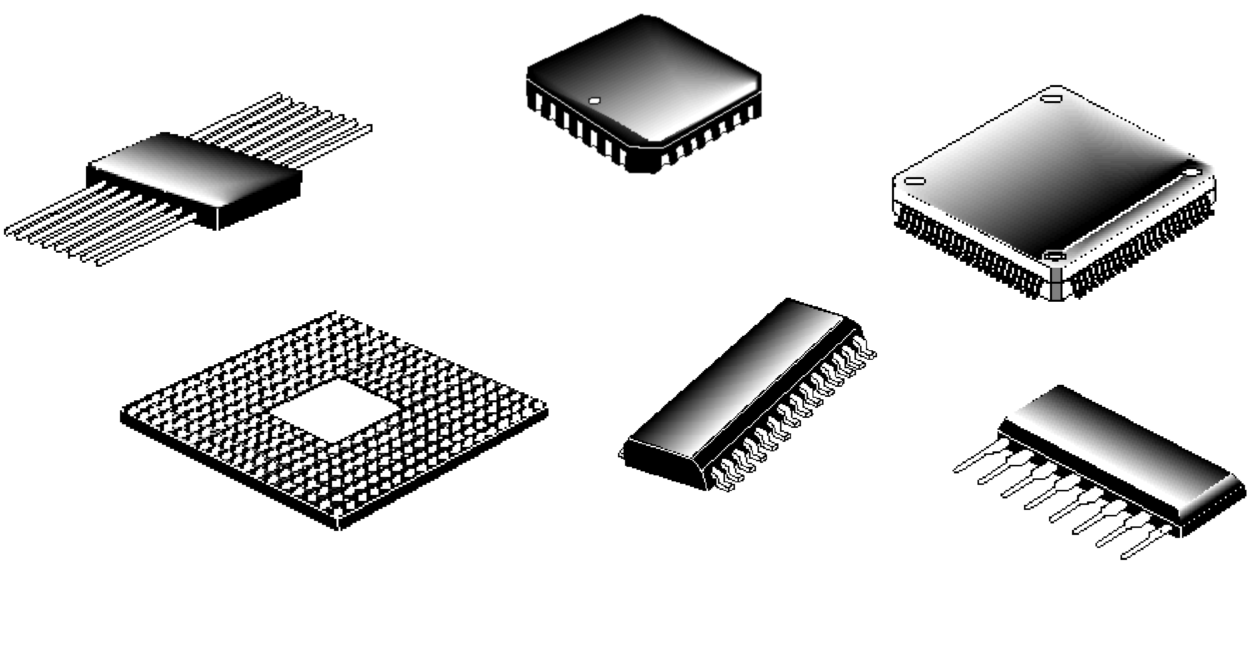
AEC - Q100 - REV-J1
March 24, 2026



FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR INTEGRATED CIRCUITS IN AUTOMOTIVE APPLICATIONS



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Revision Summary

This informative section briefly describes the changes made in the AEC-Q100 Rev-J document, compared to previous document version, AEC-Q100 Rev-H (Sept. 11, 2014). Punctuation and text improvements are not included in this summary.

- Section 1.2.1 – Automotive Reference Documents: Added reference to AEC-Q006, added AEC-Q100 sub specifications to list of references for clarification
- Section 1.2.3 – Industrial Reference Documents: Added reference to J-STD-002, JESD671, JEP155, JEP157, JEP178
- Section 1.2.4: Decommissioned references: Removed
- Section 1.3.1 – AEC-Q100 Qualification Statement: Guidance for ESD level reporting adapted to requirements
- NEW Section 1.3.6 – Flip-Chip Ball Grid Array (FC-BGA) Package Configuration: Added new definition for FC-BGA
- NEW Figure 1 – Illustration of a Flip-Chip BGA Package Configuration: Added new Figure illustrating FC-BGA
- NEW: Section 2.3 – Customer Specific Lifetime Requirements (Mission Profiles): Add new section to define entry point in App. 7 in main part of the document
- Section 3.3 – Criteria for Passing Qualification and Requalification: Explicitly include initial qualification
- NEW Section 3.6 – Qualification of a Device Using Copper (Cu) Wire Interconnects: Added new section on qualification of devices using Cu wire
- Section 4.3 – Wearout Reliability Tests: Added recommendation for technology qualification
- Figure 3: Adaption to changes in table 2
- Table 2 – Qualification Test Methods:
    - Column notes: added notes F, C and W to applicable tests
    - Test A1: Added delamination requirement
    - Test A2: Added interim readout test temperature requirement
    - Test A3: Added preference for UHST
    - Test A4: Change of requirement for grade 0. Added requirement for availability of delamination data
    - Test A5: Rework of trigger criteria to efficiently identify products where test is applicable
    - Test B1: Alternative TEST sequence added, drift analysis requirement added
    - Test C3: Application of J-STD-002 clarified
    - Added NEW tests C7 (BST – Bump Shear Test)
    - Test E2: Acceptance criteria for advanced CMOS nodes added
    - Test E3: Acceptance criteria for advanced CMOS nodes added
    - Table 2 Legend: Added Note C reference for Cu wire devices and Note F for FC-BGA device specific tests and Note W for devices with wires not covered in mold compound
- Table 3 – Process Change Qualification Guidelines for the Selection of Tests:
    - Added NEW Tests C7 (BST – Bump Shear Test)
    - Added NEW Wafer section and process change items Redistribution, Under Bump Metal, Bump Material, and Bump Site Transfer
- Appendix 1 – Definition of a Product Qualification Family: Complete revision
    - Section A1.3 – Assembly Process: Added reference for FC-BGA
- Appendix 2 – Q100 Certification of Design, Construction and Qualification
    - Added NEW Section 12a – Wafer Bump and sub-items UBM stack & thickness, UBM dimensions, Bump dimensions, and Bump materials
- Appendix Template 4A – AEC-Q100 Qualification Test Plan:
    - Rework to be in line with changes to table 2
- Appendix Template 4B – AEC-Q100 Generic Data:
    - Rework to be in line with changes to table 2
- Appendix 7
    - New description of the flow graphs to provide more clarity to the reader
    - Table A7.1: Clarify that this is an calculation example and not a standard condition described here

Revision Summary (continued)

This informative section briefly describes the changes made in the AEC-Q100 Rev-J1 document, compared to previous document version, AEC-Q100 Rev-J (Aug. 11, 2023). Punctuation, formation and text improvements are not included in this summary.

- Appendix 2 – Q100 Certificate of Design, Construction (CDC)
    - New Title
    - Removal of copy of old template and replacement by link to new CDC Excel based template.

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document:

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Automotive Electronics Council
Component Technical Committee

FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR INTEGRATED CIRCUITS IN AUTOMOTIVE APPLICATIONS

Text enhancements and differences made since the last revision of this document are shown as underlined areas. Several figures and tables have also been revised, but changes to these areas have not been underlined.

Unless otherwise stated herein, the date of implementation of this standard for new qualifications and re-qualifications is as of the publish date above.

1. SCOPE

This document contains a set of failure mechanism based stress tests and defines the minimum stress test driven qualification requirements and references test conditions for qualification of integrated circuits (ICs). These tests are capable of stimulating and precipitating semiconductor device and package failures. The objective is to precipitate failures in an accelerated manner compared to use conditions. This set of tests should not be used indiscriminately. Each qualification project should be examined for:

a. Any potential new and unique failure mechanisms.
b. Any situation where these tests/conditions may induce failures that would not be seen in the application.
c. Any extreme use condition and/or application that could adversely reduce the acceleration.

Use of this document does not relieve the IC supplier of their responsibility to meet their own company's internal qualification program. In this document, "user" is defined as all customers using a device qualified per this specification. The user is responsible to confirm and validate all qualification data that substantiates conformance to this document. Supplier usage of the device temperature grades as stated in this specification in their part information is strongly encouraged.

1.1 Purpose

The purpose of this specification is to determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality/reliability in the application.

1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

1.2.1 Automotive

AEC-Q001 Guidelines for Part Average Testing
AEC-Q002 Guidelines for Statistical Yield Analysis
AEC-Q003 Guidelines for Characterizing the Electrical Performance
AEC-Q004 Zero Defects Framework
AEC-Q005 Pb-Free Requirements
AEC-Q006 Qualification Requirements for Components Using Copper (Cu) Wire Interconnections
SAE J1752/3 Integrated Circuits Radiated Emissions Measurement Procedure
SAE J1879/J1211/ZVEI Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
IATF 16949 Automotive Quality Management System Standard
AIAG Production Part Approval Process (PPAP)
AEC-Q100-001 Wire Bond Shear Test
AEC-Q100-002 Human Body Model (HBM) Electrostatic Discharge Test

AEC-Q100-004 IC Latch-Up Test
AEC-Q100-005 Non-Volatile Memory Program/Erase Endurance Data Retention and Operational Life Test
AEC-Q100-007 Fault Simulation and Test Grading
AEC-Q100-008 Early Life Failure Rate (ELFR)
AEC-Q100-009 Electrical Distribution Assessment
AEC-Q100-010 Solder Ball Shear Test
AEC-Q100-011 Charged Device Model (CDM) Electrostatic Discharge Test
AEC-Q100-012 Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems

1.2.2 Military

MIL-STD-883 Department Of Defense Test Method Standard: Microcircuits

1.2.3 Industrial

JEDEC JESD22 Reliability Test Methods for Packaged Devices
UL-STD-94 Tests for Flammability of Plastic materials for parts in Devices and Appliances
IPC/JEDEC J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
IPC/JEDEC J-STD-020 Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices
JESD89 Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices
JESD89-1 System Soft Error Rate (SSER) Test Method
JESD89-2 Test Method For Alpha Source Accelerated Soft Error Rate
JESD89-3 Test Method for Beam Accelerated Soft Error Rate
JESD94 Application Specific Qualification Using Knowledge Based Test Methodology
JESD671 Component Quality Problem Analysis and Corrective Action Requirements
JEP155 Recommended ESD Target Levels for HBM Qualification
JEP157 Recommended ESD-CDM Target Levels
JEP178 Electrostatic Discharge (ESD) Sensitivity Testing – Reporting ESD Withstand Levels on Datasheets

1.3 Definitions

1.3.1 AEC Q100 Qualification

Successful completion and documentation of the test results from requirements outlined in this document allows the supplier to claim that the part is “AEC Q100 qualified”. For ESD, it is **highly recommended** that the passing HBM withstand voltage and CDM test condition are specified in the supplier datasheet with a footnote on any pin exceptions; that includes advanced CMOS nodes (28 nm and below) and RF operating frequency parts, especially if those ESD levels fall below 2kV HBM or Test Condition 750/500 CDM. A guidance on an appropriate way to report ESD withstand levels can be found in JEP178.

1.3.2 AEC Certification

Note that there are no "certifications" for AEC-Q100 qualification and there is no certification board run by AEC to qualify parts. Each supplier performs their qualification to AEC standards, considers customer requirements and submits the data to the user to verify compliance to Q100.

1.3.3 Approval for Use in an Application

"Approval" is defined as user approval for use of a part in their application. The user's method of approval is beyond the scope of this document.

1.3.4 Definition of Part Operating Temperature Grade

The part operating temperature grades are defined in Table 1 below:

Table 1: Part Operating Temperature Grades

Grade	Ambient Operating Temperature Range
0	-40°C to +150°C
1	-40°C to +125°C
2	-40°C to +105°C
3	-40°C to +85°C

The endpoint test temperatures for hot and cold test, if required for that stress test, must be equivalent to those specified for the particular grade. If accounting for junction heating during powered test, hot test endpoint test temperature can be greater.

For Test Group B – Accelerated Lifetime Simulation Tests: High Temperature Operating Life (HTOL), Early Life Failure Rate (ELFR) and NVM Endurance, Data Retention, and Operational Life (EDR), the junction temperature of the device during stressing should be equal to or greater than the hot temperature for that grade.

1.3.5 Capability Measures Cpk

Refer to AEC-Q003 Characterization to understand how the Cpk measure will be used in this standard.

1.3.6 Flip-Chip Ball Grid Array (FC-BGA) Package Configuration

Figure 1 shows two representative package configurations where a bare die is attached to a substrate via bumps or pillars (other possible configurations may apply). The package may also utilize a lid (e.g., heat-spreader) or be encapsulated using a plastic molding compound. The substrate includes solder balls that serve as the interface to a printed circuit board.

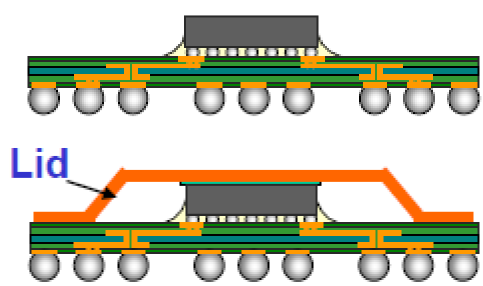


Figure 1: Representative Illustration of a Flip-Chip BGA Package

2. GENERAL REQUIREMENTS

2.1 Objective

The objective of this specification is to establish a standard that defines operating temperature grades for integrated circuits based on a minimum set of qualification requirements.

2.1.1 Zero Defects

Qualification and some other aspects of this document are a subset of, and contribute to, the achievement of the goal of Zero Defects. Elements needed to implement a zero defects program are described in AEC-Q004 Zero Defects Framework.

2.2 Precedence of Requirements

In the event of conflict in the requirements of this standard and those of any other documents, the following order of precedence applies:

a. The purchase order (or master purchase agreement terms and conditions)
b. The (mutually agreed) individual device specification
c. This document
d. The reference documents in Section 1.2 of this document
e. The supplier's data sheet

For the device to be considered a qualified part per this specification, the purchase order and/or the individual device specification cannot waive or detract from the requirements of this document.

2.3 Customer Specific Lifetime Requirements (Mission Profiles)

If the user requires a qualification to cover a specific mission profile, the flow chart in Appendix 7 can be used to determine the qualification strategy either with a standard test plan per Table 2 or a modified test plan.

Appendix 7 applies the base elements of Knowledge-Based-Test-Methodology (KBTM) and provides guidance for which element of KBTM should be used. Please refer to JESD94 on KBTM approach. KBTM can be applied on certain cases for qualification when appropriately communicated between suppliers and users.

2.4 Use of Generic Data to Satisfy Qualification and Requalification Requirements

2.4.1 Definition of Generic Data

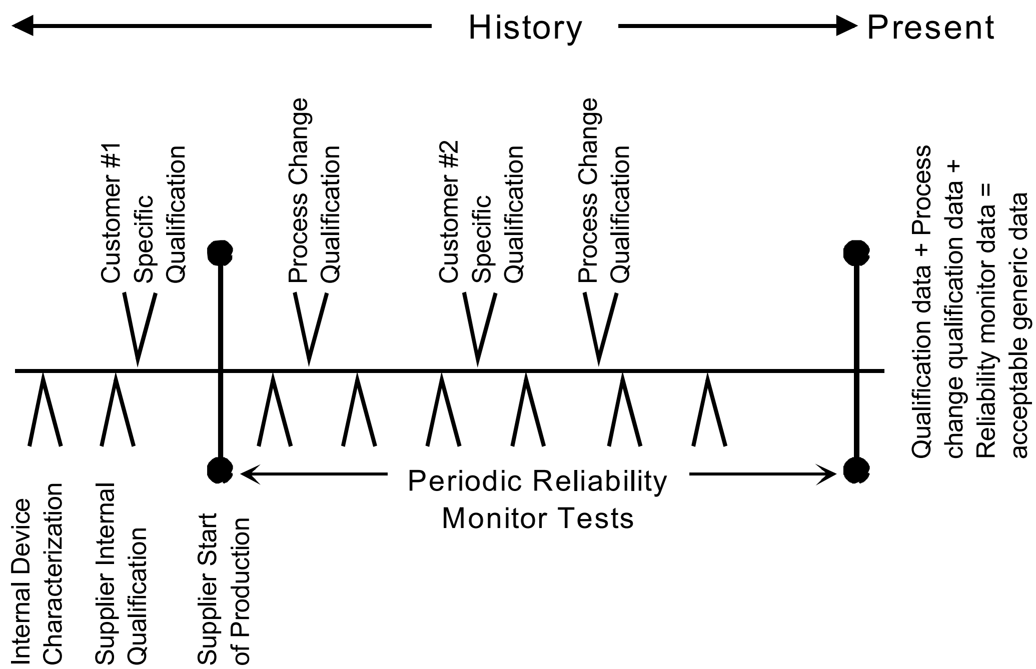
The use of generic data to simplify the qualification process is strongly encouraged. Generic data can be submitted to the user as soon as it becomes available to determine the need for any additional testing. To be considered, the generic data must be based on a matrix of specific requirements associated with each characteristic of the device and manufacturing process as shown in Table 3 and Appendix 1. **If the generic data contains any failures, the data is not usable as generic data unless the supplier has documented and implemented corrective action or containment for the failure condition that is acceptable to the user.**

Appendix 1 defines the criteria by which components are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable for the qualification of the device in question. For each stress test, two or more qualification families can be combined if the reasoning is technically sound (i.e., supported by data).

Table 3 defines a set of qualification tests that must be considered for any changes proposed for the component. The Table 3 matrix is the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and user should use as a baseline for discussion of tests that are required for the qualification in question. **It is the supplier's responsibility to present a rationale for why any of the listed tests need not be performed.**

2.4.2 Time Limit for Acceptance of Generic Data

There are no time limits for the acceptability of generic data. Use the diagram below for appropriate sources of reliability data that can be used. This data must come from the specific part or a part in the same qualification family, as defined in Appendix 1. Potential sources of data could include any customer specific data (withhold customer name), process change qualification, and periodic reliability monitor data (see Figure 2).



Note: Some process changes (e.g., die shrink) will affect the use of generic data such that data obtained before these types of changes will not be acceptable for use as generic data.

Figure 2: Generic Data Time Line

2.5 Test Samples

2.5.1 Lot Requirements

Test samples shall consist of a representative device from the qualification family. Where multiple lot testing is required due to a lack of generic data, test samples as indicated in Table 2 must be composed of approximately equal numbers from non-consecutive wafer lots, assembled in non-consecutive assembly lots. That is, they must be separated in the fab or assembly process line by at least one non-qualification lot. Any deviation from the above requires technical explanation from the supplier.

2.5.2 Production Requirements

All qualification devices shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at production volumes. Other electrical test sites may be used for electrical measurements after their electrical quality is validated.

2.5.3 Reusability of Test Samples

Devices that have been used for nondestructive qualification tests may be used to populate other qualification tests. Devices that have been used for destructive qualification tests may not be used any further except for engineering analysis.

2.5.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 2.

If the supplier elects to use generic data for qualification, the specific test conditions and results must be recorded and available to the user (preferably in the format shown in Appendix 4). Existing applicable generic data should first be used to satisfy these requirements and those of Section 2.4 for each test requirement in Table 2. Device specific qualification testing should be performed if the generic data does not satisfy these requirements.

2.5.5 Pre- and Post-stress Test Requirements

Test temperatures both pre- and post-stress (room, hot and/or cold) are specified in the "Additional Requirements" column of Table 2 for each test.

2.6 Definition of Test Failure After Stressing

Test failures are defined as those devices not meeting the individual device specification, criteria specific to the test, or the supplier's data sheet, in the order of significance as defined in Section 2.2. Any device that shows external physical damage attributable to the environmental test is also considered a failed device. If the cause of failure is due to mishandling during stressing or testing such as EOS or ESD, or some other cause unrelated to the component reliability, the failure shall be discounted but reported as part of the data submission.

3. QUALIFICATION AND REQUALIFICATION

3.1 Qualification of a New Device

The stress test requirement flow for qualification of a new device is shown in Figure 3 with the corresponding test conditions defined in Table 2. For each qualification, the supplier must have data available for all of these tests, whether it is stress test results on the device to be qualified or acceptable generic data. A review shall also be made of other devices in the same generic family to ensure that there are no common failure mechanisms in that family. Detailed justification for the use of generic data shall be communicated and explicitly reported by the supplier.

For each device qualification, the supplier must have available the following:

- Certificate of Design, Construction and Qualification (see Appendix 2)
- Stress Test Qualification data (see Table 2 & Appendix 4)
- Data indicating the level of fault grading of the test software used for qualification (when applicable to the device type) per Q100-007 that will be made available to the user upon request

3.2 Requalification of a Changed Device

Requalification of a device is required when the supplier makes a change to the product and/or process that impacts (or could potentially impact) the form, fit, function, quality and/or reliability of the device (see Table 3 for guidelines).

3.2.1 Process Change Notification

The supplier will meet the user requirements for product/process changes.

3.2.2 Changes Requiring Requalification

As a minimum, any change to the product, as defined in Appendix 1, requires performing the applicable tests listed in Table 2, using Table 3 to determine the requalification test plan. Table 3 should be used as a guide for determining which tests are applicable to the qualification of a particular part change or whether equivalent generic data can be submitted for that test(s).

3.3 Criteria for Passing Qualification and Requalification

All failures shall be analyzed for root cause. **Only when corrective and preventative actions are in place, have been proven effective for valid failures, and the 8D methodology (Eight Discipline, see JESD671) has been completed, the part may then be considered AEC Q100 qualified.** The supplier is responsible for proving the effectiveness of its 8D.

3.4 User Approval

User approval will be per IATF 16949, applicable customer specific requirements, or AIAG PPAP requirements and is outside the scope of this document.

3.5 Qualification of a Pb-Free Device

Added requirements needed to address the special quality and reliability issues that arise when Lead (Pb)-Free processing is utilized is specified in AEC-Q005 Pb-Free Requirements. Materials used in Pb-Free processing include the termination plating and the board attach (solder). These new materials usually require higher board attach temperatures to yield acceptable solder joint quality and reliability. These higher temperatures may adversely affect the moisture sensitivity level of plastic packaged semiconductors. As a result, new, more robust mold compounds may be required. If an encapsulation material change is required to provide adequate robustness for Pb-Free processing of the device, the supplier should refer to the process change qualification requirements in this specification. Preconditioning should be performed at the Pb-free reflow classification temperatures described in IPC/JEDEC J-STD-020 Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices before environmental stress tests.

3.6 Qualification of a Device Using Copper (Cu) Wire Interconnects

Devices using Copper (Cu) wire shall have supporting data according AEC-Q006.

4. QUALIFICATION TESTS

4.1 General Tests

Test flows are shown in Figure 3 and test details are given in Table 2. Not all tests apply to all devices. For example, certain tests apply only to ceramic packaged devices, others apply only to devices with NVM, and so on. The applicable tests for the particular device type are indicated in the "Note" column of Table 2. The "Additional Requirements" column of Table 2 also serves to highlight test requirements that supersede those described in the referenced test method. Any unique qualification tests or conditions requested by the user and not specified in this document shall be negotiated between the supplier and user requesting the test.

4.2 Device Specific Tests

The following tests must be performed. Generic data is not allowed for these tests. Device specific data, if it already exists, is acceptable.

1. Electrostatic Discharge (ESD) - All product.

2. Latch-up (LU) - All product.

3. Electrical Distribution - All product. The supplier must demonstrate, over the operating temperature grade, voltage, and frequency, that the device is capable of meeting the parametric limits of the device specification. This data must be taken from at least three lots, or one matrixed (or skewed) process lot, and must represent enough samples to be statistically valid, see Q100-009. It is strongly recommended that the final test limits be established using AEC-Q001 Guidelines For Part Average Testing.

4.3 Wearout Reliability Tests

Typically a product qualification according to this document is not sufficient to release a new technology for manufacturing of automotive products. It is highly recommended to perform a technology qualification using knowledge based methodologies as prerequisite to the product qualification.

Testing for the failure mechanisms listed below must be available to the user whenever a new technology or material relevant to the appropriate wearout failure mechanism is to be qualified. The data, test method, calculations, and internal criteria need not be demonstrated or performed on the qualification of every new device, but should be available to the user upon request.

- Electromigration
- Time-Dependent Dielectric Breakdown (or Gate Oxide Integrity Test) - for all MOS technologies
- Hot Carrier Injection - for all MOS technologies below 1 micron
- Bias Temperature Instability - for all CMOS below 1 micron for NBTI and PBTI as appropriate
- Stress Migration

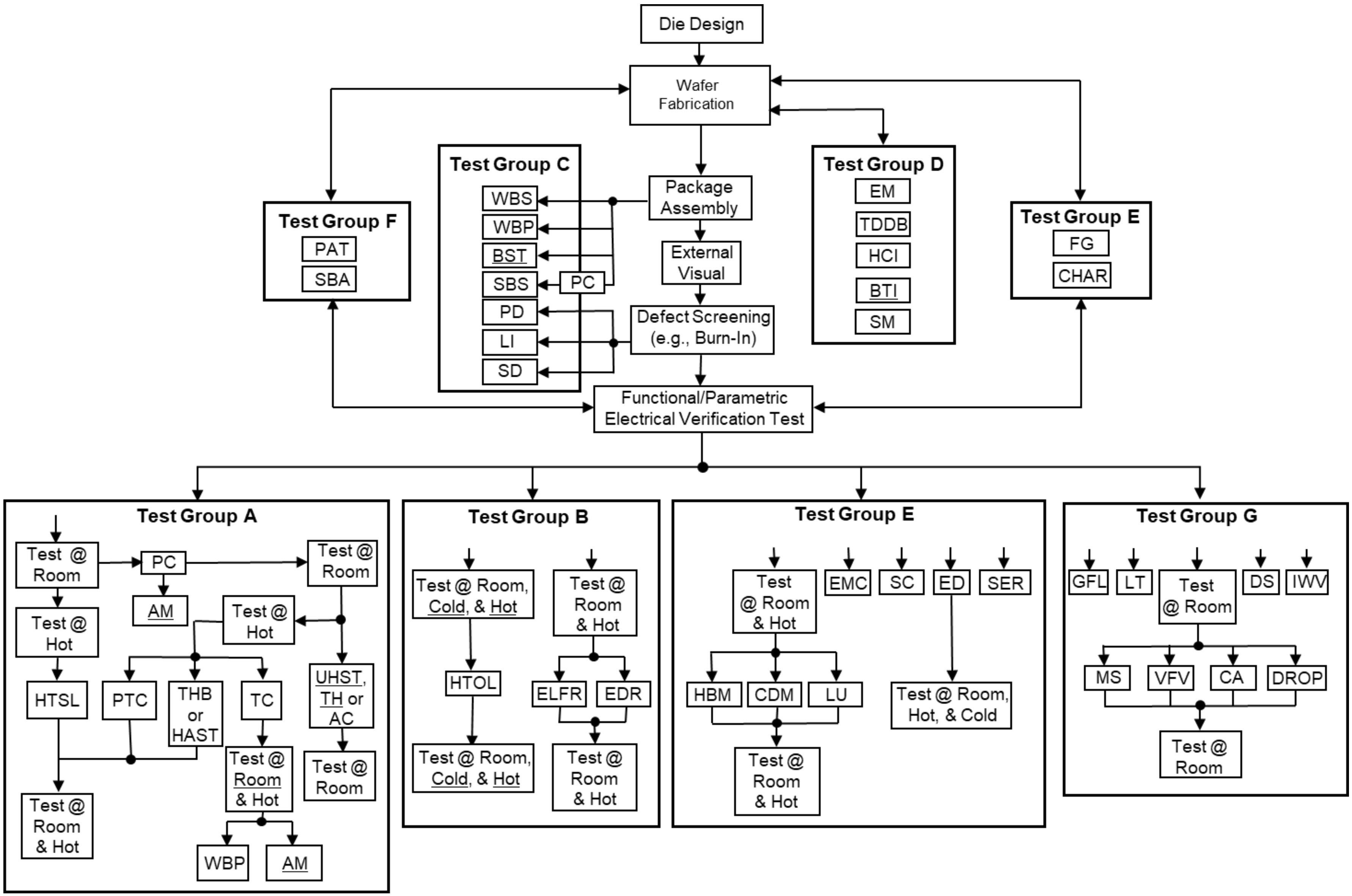


Figure 3: Qualification Test Flow

Table 2: Qualification Test Methods

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
STRESS	**ABV**	**#**	**NOTES**	**SAMPLE SIZE / LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
Preconditioning	**PC**	A1	P, B, S, G, C, F	77	3	0 Fails	JEDEC J-STD-020 JESD22-A113	Performed on surface mount devices only. PC performed before THB/HAST, AC/UHST/TH, TC, and PTC stresses. It is recommended that J-STD-020 be performed to determine what preconditioning level to perform in the actual PC stress per JESD22-A113. The minimum acceptable level for qualification is level 3 per JESD22-A113. Where applicable, preconditioning level and Peak Reflow Temperature must be reported when preconditioning and/or MSL is performed. Delamination from the die surface in JESD22-A113/J-STD-020 is acceptable if the device passes the subsequent Qualification tests. Any replacement of devices must be reported. Check 3 devices each from 3 lots (9 devices in total) for delamination via AM (Acoustic Microscopy) after PC. Die attach delamination greater than 50% for active die attach (electrically or thermally active) must be reported. Wire bonding surface delamination must be reported. **TEST before and after PC at room temperature.**
Temperature-Humidity-Bias or Biased HAST	**THB or HAST**	A2	P, B, D, G, C, F	77	3	0 Fails	JEDEC JESD22-A101 or A110	For surface mount devices, PC before THB (85°C/85%RH for 1000 hours) or HAST (130°C/85%RH for 96 hours, or 110°C/85%RH for 264 hours). **TEST before and after THB or HAST at room and hot temperature (in that order). Intermediate read points to be tested at room temperature only.**
Autoclave or Unbiased HAST or Temperature-Humidity (without Bias)	**AC or UHST or TH**	A3	P, B, D, G, F	77	3	0 Fails	JEDEC JESD22-A102, A118, or A101	For surface mount devices, PC before AC (121°C/15psig for 96 hours) or unbiased HAST (130°C/85%RH for 96 hours, or 110°C/85%RH for 264 hours). UHST is strongly preferable to AC. For packages sensitive to high temperatures and pressure (e.g., BGA), PC followed by TH (85°C/85%RH) for 1000 hours may be substituted. **TEST before and after AC, UHST, or TH at room temperature.**

Table 2: Qualification Test Methods (continued)

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (CONTINUED)								
STRESS	**ABV**	**#**	**NOTES**	**SAMPLE SIZE / LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
Temperature Cycling	**TC**	A4	H, P, B, D, G, C, F	77	3	0 Fails	JEDEC JESD22-A104 and Appendix 3	PC before TC for surface mount devices. **Grade 0:** -55ºC to +150ºC for 1500 cycles or equivalent. **Grade 1:** -55ºC to +150ºC for 1000 cycles or equivalent. **Note:** -65ºC to 150ºC for 500 cycles is also an allowed test condition due to legacy use with no known lifetime issues. **Grade 2:** -55ºC to +125ºC for 1000 cycles or equivalent. **Grade 3:** -55ºC to +125ºC for 500 cycles or equivalent. **TEST before and after TC at room and hot temperature.** After completion of TC, decap five devices from one lot and perform WBP (test #C2) on corner bonds (2 bonds per corner) and one mid-bond per side ***on each device***. Preferred decap procedure to minimize damage and chance of false data is shown in Appendix 3. **To be implemented on or before Feb, 1st, 2024:** Check 3 devices each from 3 lots (9 devices in total) for delamination in die attach (if electrically or thermally active) or wire bonding surface areas via AM (Acoustic Microscopy) after TC. The results shall be provided to the user upon request.
Power Temperature Cycling	**PTC**	A5	H, P, B, D, G, C, F	45	1	0 Fails	JEDEC JESD22-A105	PC before PTC for surface mount devices. Test required only on devices used in applications where repetitive changes in power dissipation ≥ 1 watt and power rise times < 0.1s resulting in junction temperature changes ≥ 40ºC are anticipated (e.g., smart power switches for inductive loads). **Grade 0:** T_a of -40ºC to +150ºC for 1000 cycles. **Grade 1:** T_a of -40ºC to +125ºC for 1000 cycles. **Grades 2 and 3:** T_a -40ºC to +105ºC for 1000 cycles. Thermal shut-down shall not occur during this test. **TEST before and after PTC at room and hot temperature.**
High Temperature Storage Life	**HTSL**	A6	H, P, B, D, G, K, C, F	45	1	0 Fails	JEDEC JESD22-A103	**Plastic Packaged Parts and Flip-Chip BGAs** **Grade 0:** +175ºC T_a for 1000 hours or +150ºC T_a for 2000 hours. **Grade 1:** +150ºC T_a for 1000 hours or +175ºC T_a for 500 hours. **Grades 2 and 3:** +125ºC T_a for 1000 hours or +150ºC T_a for 500 hours. **Ceramic Packaged Parts** +250ºC T_a for 10 hours or +200ºC T_a for 72 hours. **TEST before and after HTSL at room and hot temperature.** *** NOTE: Data from Test B3 (EDR) can be substituted for Test A6 (HTSL) if package and grade level requirements are met.**

Table 2: Qualification Test Methods (continued)

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS								
STRESS	**ABV**	**#**	**NOTES**	**SAMPLE SIZE / LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
High Temperature Operating Life	**HTOL**	B1	H, P, B, D, G, K, F	77	3	0 Fails	JEDEC JESD22-A108	For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005. **Grade 0:** +150ºC T_a for 1000 hours. **Grade 1:** +125ºC T_a for 1000 hours. **Grade 2:** +105ºC T_a for 1000 hours. **Grade 3:** +85ºC T_a for 1000 hours. HTOL NOTES: 1) HTOL stress times for the appropriate grade Ta are the min requirement; the Tj of the test (measured or calculated) should be available. 2) Tj may be used instead of Ta when performing HTOL provided that Tj of the device under HTOL conditions is equal to or higher than the Tj maximum operating (Tjopmax) of the particular device, but below the absolute maximum Tj. 3) If Tj is used to set the HTOL conditions, the minimum stress of 1000 hours at the Ta of the device is to be shown using activation energy of 0.7ev or other value technically justified. 4) V_{cc} (max) at which dc and ac parametrics are guaranteed. Thermal shut-down of the device shall not occur during this test. **TEST before and after HTOL at room, cold, and finally hot temperature (preferred). An alternate order is to test at room, hot, and finally cold temperature.** 5) If applicable, a drift analysis on the key performance and reliability related electrical parameters after HTOL should be performed to confirm a proper selection of guard bands to meet the data sheet specification. For guidance on drift analysis, refer to AEC-Q100-009.
Early Life Failure Rate	**ELFR**	B2	H, P, B, N, G, F	800	3	0 Fails	AEC Q100-008	Devices that pass this stress can be used to populate other stress tests. Generic data is applicable. **TEST before and after ELFR at room and hot temperature.**
NVM Endurance, Data Retention, and Operational Life	**EDR**	B3	H, P, B, D, G, K, F	77	3	0 Fails	AEC Q100-005	**TEST before and after EDR at room and hot temperature. Sample size and lot requirement applies to EACH of the NVM tests per Q100-005.**

Table 2: Qualification Test Methods (continued)

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS								
STRESS	**ABV**	**#**	**NOTES**	**SAMPLE SIZE / LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
Wire Bond Shear	**WBS**	C1	H, P, B, D, G, C	30 bonds from a minimum of 5 devices		C_{PK} >1.67	AEC Q100-001 AEC Q003	At appropriate time interval for each bonder to be used.
Wire Bond Pull	**WBP**	C2	H, P, B, D, G, C			C_{PK} >1.67 or 0 Fails after TC (test #A4)	MIL-STD883 Method 2011 AEC Q003	Condition C or D. For Au wire diameter ≥1mil, minimum pull strength after TC = 3 grams. For Au wire diameter <1mil, refer to Figure 2011-1 in MIL-STD-883 Method 2011 as a guideline for minimum pull strength. For Au wire diameter <1mil, wire bond pull shall be performed with the hook over the ball bond and not at mid-wire.
Solderability	**SD**	C3	H, P, B, D, G, F	15	1	per J-STD-002	JEDEC J-STD-002	If burn-in screening is normally performed on the device before shipment, samples for SD must first undergo burn-in or equivalent high temperature baking.
Physical Dimensions	**PD**	C4	H, P, B, G, F	10	3	C_{PK} >1.67	JEDEC JESD22-B100 and B108 AEC Q003	See applicable JEDEC standard outline and individual device spec for significant dimensions and tolerances.
Solder Ball Shear	**SBS**	C5	B, D, G, F	5 balls from a min. of 10 devices	3	C_{PK} >1.67	AEC Q100-010 AEC Q003	PC thermally (two reflow cycles) before integrity (mechanical) testing. Refer to J-STD-020 for Pb-free reflow profiles to be used for this test.
Lead Integrity	**LI**	C6	H, P, D, G	10 leads from each of 5 parts	1	No lead breakage or cracks	JEDEC JESD22-B105	Not required for surface mount devices. Only required for through-hole devices.
Bump Shear Test	**BST**	C7	D, F	20 bumps/pillars from a minimum of 5 devices		C_{PK} >1.67	JEDEC JESD22-B117 or equivalent AEC-Q003	JESD22-B117, Ball Shear, is a reference method. The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.

Table 2: Qualification Test Methods (continued)

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS (CONTINUED)								
STRESS	**ABV**	**#**	**NOTES**	**SAMPLE SIZE / LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
Electromigration	**EM**	D1	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.
Time Dependent Dielectric Breakdown	**TDDB**	D2	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.
Hot Carrier Injection	**HCI**	D3	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.
Bias Temperature Instability	**BTI**	D4	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.
Stress Migration	**SM**	D5	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.

Table 2: Qualification Test Methods (continued)

TEST GROUP E – ELECTRICAL VERIFICATION TESTS								
STRESS	**ABV**	**#**	**NOTES**	**SAMPLE SIZE / LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
Pre- and Post-Stress Function/Parameter	**TEST**	E1	H, P, B, N, G, F	All	All	0 Fails	Test program to supplier data sheet or user specification	Test is performed as specified in the applicable stress reference and the additional requirements in Table 2 and illustrated in Figure 2. Test software used shall meet the requirements of Q100-007. All electrical testing before and after the qualification stresses are performed to the limits of the individual device specification in temperature and limit value.
Electrostatic Discharge Human Body Model	**HBM**	E2	H, P, B, D, F	See Test Method	1	Target: 0 Fails 2KV HBM (Classification 2 or better) For ≤ 28nm or RF operating frequency: 1KV HBM (Classification 1C or better)	AEC Q100-002	**TEST before and after ESD at room and hot temperature**. Device shall be classified according to the maximum withstand voltage level and documented in the supplier qualification report. Device levels below specified targets (2KV or 1KV) require specific user approval. Refer to Section 1.3.1. Referring to a target level below 2kV (Classification 2) must be reported in the data sheet. Rationale for classifying a pin as operating at RF frequency shall be provided to the user upon request. JEDEC JEP155 can provide further guidance.
Electrostatic Discharge Charged Device Model	**CDM**	E3	H, P, B, D, F	See Test Method	1	Target: 0 Fails Test Condition 750 corner pins, Test Condition 500 all other pins (Classification C2A or better) For ≤ 28nm or RF operating frequency: Test Condition 250 (Classification C1 or better)	AEC Q100-011	**TEST before and after ESD at room and hot temperature**. Device shall be classified according to the maximum withstand test condition and documented in the supplier qualification report. Device levels below specified targets (Test Condition 500 or 250) require specific user approval. Refer to Section 1.3.1. Referring to a target level below Test Conditions 750/500 (Classification C2A) must be reported in the data sheet. Rationale for classifying a pin as operating at RF frequency shall be provided to the user upon request. JEDEC JEP157 can provide further guidance.

Table 2: Qualification Test Methods (continued)

TEST GROUP E – ELECTRICAL VERIFICATION TESTS (CONTINUED)								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Latch-Up	**LU**	E4	H, P, B, D, F	3	1	0 Fails	AEC Q100-004	See attached procedure for details on how to perform the test. **TEST before and after LU at room and hot temperature.**
Electrical Distributions	**ED**	E5	H, P, B, F	30	3	Where applicable, C_{PK} >1.67	AEC Q100-009 AEC Q003	Supplier and user to mutually agree upon electrical parameters to be measured and accept criteria. **TEST at room, hot, and cold temperature.**
Fault Grading	**FG**	E6	---	---	---	AEC Q100-007 unless otherwise specified	AEC Q100-007	For production testing, see Q100-007 for test requirements.
Characterization	**CHAR**	E7	---	---	---	---	AEC Q003	To be performed on new technologies and part families.
Electromagnetic Compatibility	**EMC**	E9	---	1	1	---	SAE J1752/3 – Radiated Emissions	See Appendix 5 for guidelines on determining the applicability of this test to the device to be qualified. This test and its accept criteria is performed per agreement between user and supplier on a case-by-case basis.
Short Circuit Characterization	**SC**	E10	D, G	10	3	0 Fails	AEC Q100-012	**Applicable to all smart power devices.** This test and statistical evaluation (see Section 4 of Q100-012) shall be performed per agreement between user and supplier on a case-by-case basis.
Soft Error Rate	**SER**	E11	H, P, D, G	3	1	---	JEDEC Un-accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3	**Applicable to devices with memory sizes ≥1Mbit SRAM or DRAM based cells.** Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications. This test and its accept criteria is performed per agreement between user and supplier on a case-by-case basis. Final test report shall include detailed test facility location and altitude data.
Lead (Pb) Free	**LF**	E12	L	See Test Method	See Test Method	See Test Method	AEC Q005	Applicable to ALL Pb-free devices. Note the recommendations for all related solderability, solder heat resistance and whisker requirements.

Table 2: Qualification Test Methods (continued)

STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
TEST GROUP F – DEFECT SCREENING TESTS								
Process Average Testing	**PAT**	F1	---	---	---	---	AEC Q001	The supplier determines the sample sizes and accept criteria per the test methods. If these tests are not possible for a given part, the supplier must provide justification. The supplier must perform some variant of PAT and SBA that meets the intent of the guideline.
Statistical Bin/Yield Analysis	**SBA**	F2	---	---	---	---	AEC Q002	
TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS								
STRESS	**ABV**	**#**	**NOTES**	**SAMPLE SIZE / LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
Mechanical Shock	**MS**	G1	H, D, G, W	15	1	0 Fails	JEDEC JESD22-B110	Y1 plane only, 5 pulses, 0.5 msec duration, 1500 g peak acceleration. **TEST before and after at room temperature.**
Variable Frequency Vibration	**VFV**	G2	H, D, G, W	15	1	0 Fails	JEDEC JESD22-B103	20 Hz to 2 KHz to 20 Hz (logarithmic variation) in >4 minutes, 4X in each orientation, 50 g peak acceleration. **TEST before and after at room temperature.**
Constant Acceleration	**CA**	G3	H, D, G, W	15	1	0 Fails	MIL-STD-883 Method 2001	Y1 plane only, 30 K g-force for <40 pin packages, 20 K g-force for 40 pins and greater. **TEST before and after at room temperature.**
Gross/Fine Leak	**GFL**	G4	H, D, G	15	1	0 Fails	MIL-STD-883 Method 1014	Any single-specified fine test followed by any single-specified gross test.
Package Drop	**DROP**	G5	H, D, G, W	5	1	0 Fails	---	Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface. This test is for MEMS cavity devices only. **TEST before and after DROP at room temperature.**
Lid Torque	**LT**	G6	H, D, G	5	1	0 Fails	MIL-STD-883 Method 2024	
Die Shear	**DS**	G7	H, D, G, W	5	1	0 Fails	MIL-STD-883 Method 2019	To be performed before cap/seal for all cavity devices.
Internal Water Vapor	**IWV**	G8	H, D, G	5	1	0 Fails	MIL-STD-883 Method 1018	

Legend for Table 2

Notes:
- **B** Required for Solder Ball Surface Mount Packaged (BGA) devices.
- **C** Test conditions and sample sizes for Cu wire devices shall be per AEC-Q006.
- **D** Destructive test, devices are not to be reused for qualification or production.
- **F** Required for Flip-Chip BGA (substrate based) packaged devices.
- **G** Generic data allowed. See Section 2.3 and Appendix 1.
- **H** Required for hermetic packaged devices.
- **K** Use method AEC-Q100-005 for preconditioning a stand-alone Non-Volatile Memory integrated circuit or an integrated circuit with a Non-Volatile Memory module.
- **L** Required for Pb-free devices.
- **N** Nondestructive test, devices can be used to populate other tests or they can be used for production.
- **P** Required for plastic packaged devices.
- **S** Required for surface mount plastic packaged devices.
- **W** Required for wire bonded die only without overmolding at the wire.

Reference Number for the particular test.

* All electrical testing before and after the qualification stresses are performed to the limits of the individual device specification in temperature and limit value.

Table 3: Process Change Qualification Guidelines for the Selection of Tests

A2 Temperature Humidity Bias / HAST
A3 Autoclave / Unbiased HAST
A4 Temperature Cycling
A5 Power Temperature Cycling
A6 High Temperature Storage Life
B1 High Temperature Operating Life
B2 Early Life Failure Rate
B3 NVM Endurance, Data Retention
C1 Wire Bond Shear
C2 Wire Bond Pull
C3 Solderability
C4 Physical Dimensions
C5 Solder Ball Shear
C6 Lead Integrity
C7 Bump Shear
D1 Electromigration
D2 Time Dependent Dielectric Breakdown
D3 Hot Carrier Injection
D4 Bias Temperature Instability
D5 Stress Migration
E2 Human Body Model ESD
E3 Charged Device Model ESD
E4 Latch-up
E5 Electrical Distribution
E7 Characterization
E9 Electromagnetic Compatibility
E10 Short Circuit Characterization
E11 Soft Error Rate
E12 Pb-Free
G1-G4 Mechanical Series
G5 Package Drop
G6 Lid Torque
G7 Die Shear
G8 Internal Water Vapor

Note: A letter or "●" indicates that performance of that stress test should be **considered** for the appropriate process change. Reason for not performing a considered test should be given in the qualification plan or results.

Table 2 Test #	A2	A3	A4	A5	A6	B1	B2	B3	C1	C2	C3	C4	C5	C6	C7	D1	D2	D3	D4	D5	E2	E3	E4	E5	E7	E9	E10	E11	E12	G1-G4	G5	G6	G7	G8
Test Abbreviation	THB	AC	TC	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	PD	SBS	LI	BST	EM	TDDB	HCI	BTI	SM	HBM	CDM	LU	ED	CHAR	EMC	SC	SER	LF	MECH	DROP	LT	DS	IWV
DESIGN																																		
Active Element Design		●	●	M		●	●	DJ								D	D	D	D	D	●	●	●	●	●	●	●	●			F			
Circuit Rerouting			A	M																	●	●	●	●	●	●	●							
Wafer Dimension/ Thickness			E	M		●	●		E	E									●		E	E	E	●										
WAFER FAB																																		
Lithography	●		●	M		●	G		●	●									●					●										
Die Shrink	●	●		M		●	●	DJ								●	●	●	●	●	●	●	●	●	●	●	●	●						
Diffusion/Doping				M		●	G												●		●	●	●	●	●									
Polysilicon			●	M		●		DJ											●		●	●	●	●	●									
Metallization/Via/ Contacts	●	●	●	M		●			●	●						●				●				●	●		●							
Passivation/Oxide/ Interlevel Dielectric	K	K	●	M		●	GN	DJ	K	●							●	●	●	●	●	●	●	●	●									
Backside Operation			●	M		●															M	M	●		●					H			H	
FAB Site Transfer	●	●	●	M		●	●	J	●	●						●	●	●	●	●	●	●	●	●						H			H	
WAFER BUMPING																																		
Redistribution Layer	●	●	●	M	●										●									●										
Under Bump Metal	●	●	●	M	●										●									●										
Bump Material	●	●	●	M	●										●									●										
Bump Site Transfer	●	●	●	M	●										●									●										
ASSEMBLY																																		
Die Overcoat/ Underfill	●	●	●	M	●	●																						●						H
Leadframe Plating	●	●	●	M	●					C	●			●															L				H	
Bump Material/ Metal System	●	●	●	M	●	●						●	●															●	L					
Leadframe Material		●	●	M	●					●	●	●		●													●		L	H			H	
Leadframe Dimension		●	●	M							●	●		●													●		L	H				
Wire Bonding	●	●	●	Q	●				●	●														M			●			H				
Die Scribe/ Separate	●	●	●	M																														
Die Preparation/ Clean	●	●		M		●			●	●																							H	
Package Marking											B																							
Die Attach	●	●	●	M		●																		●			●		L	H			H	H
Molding Compound	●	●	●	M	●	●	●				●	●		●														●	L					
Molding Process	●	●	●	M	●	●					●	●		●															L					
Hermetic Sealing		H	H		H							H		H																H		H		H
New Package	●	●	●	M	●	●	●		●	●	●	●	T	●							●	●		●			●		L	H			H	H
Substrate/Interposer	●	●	●	M	●	●			●	●			T																L	H			H	H
Assembly Site Transfer	●	●	●	M		●	●		●	●	●	●	T	●										●					L	H			H	H

A Only for peripheral routing
B For symbol rework, new cure time, temp
C If bond to leadfinger
D Design rule change
E Thickness only
F MEMS element only
G Only from non-100% burned-in parts
H Hermetic only
J EPROM or E^2PROM
K Passivation only
L For Pb-free devices only
M For devices requiring PTC
N Passivation and gate oxide
Q Wire diameter decrease
T For Solder Ball SMD only

Appendix 1: Definition of a Product Qualification Family

AECQ100 provides the following guideline for use of generic data to accelerate and streamline the qualification process for suppliers and users. Suppliers and users can use this guideline to reach mutual agreement on how to utilize generic data when it is appropriate.

For devices to be categorized in a product qualification family, they all must share the same major product, process and materials elements as defined below. The qualification of a particular product will be defined within, but not limited to, the categories listed below. Critical product functional details as defined in Section A1.1 and critical process steps and materials as defined in Sections A1.2 and A1.3 do not need to be matched exactly, but shall cover worst cases in application of the family generic data through technical justification.

All products in the same product qualification family are qualified by association when one family member successfully completes qualification with the exception of the device specific requirements of Section 4.2.

For broad changes that involve multiple attributes (e.g., site, materials, processes), refer to Section A1.5 of this appendix and Section 2.4 of Q100, which allows for the selection of worst-case test vehicles to cover all the possible permutations.

A1.1 Product

a. Product functionality (e.g., Op-Amp, regulator, microprocessor, Logic - HC/TTL)
b. Operating supply voltage range(s)
c. Specified operating temperature range
d. Specified operating frequency range
e. Design library cells for the fab technology
   - Memory IP (e.g., cell structure, building block)
   - Digital design library cells (e.g., circuit blocks, IO modules, ESD cells) and/or analog design library cells (e.g., active circuit elements, passive circuit elements) at data sheet voltage level(s) and at data sheet or better temperature range, and power dissipation
   - Speed/performance of the library cells
f. Memory type(s) and sizes
g. Design rules for active circuits under pads
h. Other functional characteristics as defined by supplier

For parts specified to operate at different power supplies (e.g., 5.0 V and 3.3 V), product qualification family data should be presented for both supply ranges.

For parts specified to operate at different temperature ranges, three (3) lots of data from the product qualification family at the temperature of the device in the data sheet need to be presented with Table 2 E1 TEST data. Stress classification at the temperature specified in Q100 Table 2 groups A, B, E, and G must be equal to or higher than the device qualified. Three (3) lots of data from the product family at the frequency of the device in the data sheet need to be presented with Table 2 E1 TEST data at the temperature specified in Q100 Table 2 groups A, B, E, and G. All memory types must be demonstrated to be qualified over three (3) lots using largest memory size to be qualified for devices in the family. If the part to be qualified has a larger memory size than the one already qualified, the supplier must perform at least one lot of testing on the larger memory configuration.

A1.2 Fab Process

Each process technology (e.g., CMOS, NMOS, Bipolar) must be considered and qualified separately. No matter how similar, processes from one fundamental fab technology cannot be used for another. For BiCMOS devices, data must be taken from the appropriate technology based on the circuit under consideration.

"Worst case" family requalification with the appropriate tests is required when the process or a material is changed (see Table A1.1 and Table A1.2 for guidelines). The important attributes defining a fab process are listed below:

a. **Wafer Fab Technology** (e.g., CMOS, NMOS, Bipolar)

b. **Wafer Fab Process** - consisting of the same attributes listed below:
- Circuit element feature size (e.g., layout design rules, die shrinks, contacts, gates, isolations)
- Substrate (e.g., orientation, doping, epi, wafer size)
- Number of masks (supplier must show justification for waiving this requirement)
- Lithographic process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)
- Doping process (e.g., diffusion vs. ion implantation)
- Gate structure, material and process (e.g., polysilicon, metal, salicide, wet vs. dry etch)
- Polysilicon material, thickness range & number of levels
- Oxidation process and thickness range (e.g., gate & field oxides)
- Interlayer dielectric material & thickness range
- Metallization material, thickness range & number of levels
- Passivation process (e.g., passivation oxide opening), material, & thickness range
- Die backside preparation process & metallization

c. **Wafer Fab Site**

A1.3 Assembly Process – Plastic, Ceramic, or Flip-Chip BGA

The processes for plastic and ceramic package technologies must be considered and qualified separately. For devices to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification with the appropriate tests is required when the process or a material is changed. The supplier must submit technical justification to the user to support the acceptance of generic data with pin (ball) counts, die sizes, substrate dimensions/material/thickness, paddle sizes and die aspect ratios different than the device to be qualified. The supplier must possess technical data to justify the acceptance of generic data. The important attributes defining a qualification family are listed below:

a. **Package Type** (e.g., DIP, SOIC, PLCC, QFP, PGA, PBGA, FC-BGA)
- Worst case within same package type (e.g., package warpage due to coefficients of thermal expansion mismatch)
- Range of paddle (flag) size (maximum & minimum dimensions) qualified for the die size/aspect ratio under consideration
- Substrate base material (e.g., PBGA, FC-BGA)
- Non-packaged devices (e.g., bare die, WL-CSP) are outside the scope of this section.

b. **Assembly Process** - consisting of the same attributes listed below:
- Leadframe base material
- Leadframe plating process & material (internal & external to the package)
- Die header / Thermal pad material
- Die attach material
- Wire bond material & diameter
- Wire bond method, presence of downbonds, & process

- Plastic mold compound material, organic substrate material, or ceramic package material
- Solder Ball metallization system (if applicable)
- Heatsink type, material, & dimensions
- Underfill material
- Redistribution layer, under bump metallization (UBM), and bump material
- Thermal interface material for lidded FCBGA
- Plastic Mold Compound Supplier/ID
- Die Preparation/Singulation

c. **Assembly Site**

A1.4 Qualification/Requalification Lot Requirements

Table A1.1: Part Qualification/Requalification Lot Requirements

Part Information	Lot Requirements for Qualification
New device and no applicable generic data.	Lot and sample size requirements per Table 2.
A part in a product family is qualified with 3 lots of generic data. The part to be qualified is less complex and meets the product Family Qualification Definition per Appendix 1.	Only device specific tests as defined in Section 4.2 are required. Lot and sample size requirements per Table 2 for the required tests.
A part in a product family is qualified with 3 lots of generic data. The part to be qualified is slightly more complex, with similar product functionality, meeting the product family qualification definition per Appendix 1. Examples for one (1) lot wafer / assembly qualification, would be, increasing ADC performance from 12 to 14 bits or package pin count from 16 to 20.	Review Table 3 to determine which tests from Table 2 should be considered. One (1) lot wafer / assembly lot and sample sizes per Table 2 for the required tests.
Part process change.	Review Table 3 to determine which tests from Table 2 should be considered. Lot and sample sizes per Table 2 for the required tests.
Part was environmentally tested to all the test extremes, but was electrically end-point tested at a temperature less than the Grade required.	The electrical end-point testing on at least 3 lots (that completed qualification testing) must meet or exceed the temperature extremes for the device Grade required. Sample sizes shall be per Table 2.
Qualification/Requalification involving multiple sites.	Refer to Appendix 1, Section A1.5.
Qualification/Requalification involving multiple families.	Refer to Appendix 1, Section A1.5.

Table A1.2: Examples for Generic Data Use

The cases listed in the generic data portion of the table signify those scenarios in which a product and site combination has been previously qualified and generic data exists. The use options of generic data described in each case define the allowable generic data for device A_n in the qualification portion of the table.

Guidelines for using Table A1.2:

1. Product A_n is a product to be qualified that belongs to Product Family A.
2. Product A_1 should be representative of the product family, possibly a more complex case family part (e.g., 60V regulator vs. 45V regulator, 8 channel vs. 4 channel amplifier) that would cover most, if not all, other family parts.
3. Same Fab is same process node and materials. Different Fab has one or more different process elements.
4. Same Assembly is same process, materials and package type. Different Assembly has one or more different process, material elements or package elements.
5. New test is qualification tests per Section 4.1
6. Fab process C_1 is the same as C except for one or more different elements (e.g., Al to Cu metal).
7. Assembly process E_1 is the same as E except for one or more different elements (e.g. Al to Cu bond wire, mold compound).
8. Product B is functionally different from Product A (e.g., logic vs. analog, voltage regulator vs. amplifier).
9. Increased product complexity can decrease the applicability for portion of the table below.

New Qualification Scenario (Definition of Part to be Qualified)

Case	Description	Product	Fab Site	Assembly Site	Min. Lots of Data Needed for Qualification	Product/Process (defined in Appendix A1)
New Device / Product	This is the unqualified device / product	A_n	C	E	3	• 1 lot ESD and LU; 3 lots ED AC(E) and 1 lot HTOL minimum on A_nCE in addition to below for all cases

Previously Qualified Scenario (Existing Generic Data)

Case	Description	Product	Fab Site	Assembly Site	Lots of Generic Data Available	Use Options of Generic Data
1	B from a different product family	B	C	E	3	**No Option** • 3 lots A_nCE (new test)
2A	B from a different product family	B	C	F	3	**No Option** • 3 lots using A_n (new test)
2B			D	E	3	**No Option** • 3 lots A_nCE (new test)
3	Different Fab Process and different site as A_1 Different Assembly and different site as A_1	A_1	D	F	3	**No Option** • 3 lots using A_n (new test)

Table A1.2: Examples for Generic Data Use (Continued)

Previously Qualified Scenario (Existing Generic Data) (continued)

Case	Description	Product	Fab Site	Assembly Site	Lots of Generic Data Available	Use Options of Generic Data
4A	One or more elements of the fab process is different than the base process Same Assembly Process and site as A_1	A_1	C_1	E	3	• 3 lots A_nCE (new test) **OR** • 2 lots A_nCE (new test) + 2 lots A_1C_1E (generic) **OR** • 1 lot A_nCE (new test) + 3 lots A_1C_1E (generic)
4B	Same Fab Process and same site as A_1 One or more elements of the assembly process is different than the base process E		C	E_1	3	• 3 lots A_nCE (new test) **OR** • 2 lots A_nCE (new test) + 2 lots A_1CE_1 (generic) **OR** • 1 lot A_nCE (new test) + 3 lots A_1CE_1 (generic)
5A	Same Fab Process and site as A_n Same Assembly Process but different site as A_n	A_1	C	F	3	• 3 lots A_nCE (new test) **OR** • 2 lots A_nCE (new test) + 2 lots A_1CF (generic) **OR** • 1 lot A_nCE (new test) + 3 lots A_1CF (generic)
5B	Same Fab Process, but different site as A_n Same Assembly Process and site as A_n		D	E	3	• 3 lots A_nCE (new test) **OR** • 2 lots A_nCE (new test) + 2 lots A_1DE (generic) **OR** • 1 lot A_nCE (new test) + 3 lots A_1DE (generic)
6	Same Fab Process and site as A_n Same Assembly Process and site as A_n	A_1	C	E	3	• 3 lots A_1CE (Generic)

A1.5 Qualification of Changes in Multiple Sites and Families

A1.5.1 Multiple Sites

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

A1.5.2 Multiple Families

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab family or assembly family, the qualification test vehicles should be: 1) One lot of a single device type from each of the families that are projected to be most sensitive to the changed attribute, or 2) Three lots total (from any combination of acceptable generic data and stress test data) from the most sensitive families if only one or two families exist.

Below is the recommended process for qualifying changes across many process and product families:

a. Identify all products affected by the proposed process changes.

b. Identify the critical structures and interfaces potentially affected by the proposed process change.

c. Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces (see the example in Table A1.3). Note that steps (a) to (c) are equivalent to the creation of an FMEA.

d. Define the product groupings or families based upon similar characteristics as they relate to the structures and device sensitivities to be evaluated, and provide technical justification to document the rationale for these groupings.

e. Provide the qualification test plan, including a description of the change, the matrix of tests, and the representative products that will address each of the potential failure mechanisms and associated failure modes.

f. Robust process capability must be demonstrated at each site (e.g., control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process steps.

Table A1.3: Example of Failure Mode/Mechanism List for a Passivation Change

Critical Structure or Interface	Potential Failure Mechanism	Associated Failure Modes	On These Products
Passivation to Mold Compound Interface	Passivation Cracking - Corrosion	Functional Failures	All Die
	Mold Compound - Passivation Delamination	Corner Wire Bond Failures	Large Die
Passivation to Metallization Interface	Stress-Induced Voiding	Functional Failures	Die with Minimum Width Metal Lines
	Ionic Contamination	Leakage, Parametric Shifts	All Die
Polysilicon and Active Resistors	Piezoelectric Leakage	Parametric Shifts (e.g., Resistance, Gain, Offset)	Analog Products

Appendix 2: Q100 Certification of Design & Construction (CDC)

When documenting a device has met the requirements of AEC-Q100, it is necessary to provide information on the construction and processing of the device. This information is provided in a CDC (Certification of Design & Construction) document. The CDC details the major manufacturing locations, material components and design characteristics.

AEC has developed a template that includes all information related to a component containing one or more integrated circuits (ICs). This template can be downloaded from the AEC website at http://www.aecouncil.com. While use of this template is not required, it is recommended as it contains all requested information as well as instructions, guidelines and helpful information (see comments in template for details). If this template is not used, it is up to the IC supplier to provide the information in an alternate format.

All fields in the template should be filled out as completely as possible. Each data entry has information on the format of the field and how each entry should be completed. If a field cannot be entered because it does not apply, it should be filled as “Not Applicable”. If a field cannot be filled due to proprietary or other reasons, it should be filled as “Unavailable”

The top portion of the “Overview – Signature” page of the CDC Template is shown below:

Automotive Electronics Council
Component Technical Committee

AEC-Q100 Integrated Circuit (IC) Certificate of Design & Construction (CDC) Template

The following information is used to document construction of an Integrated Circuit (IC) conforming to AEC-Q100. The use of this template is optional, though encouraged as this document was developed to meet Automotive Tier 1 user requirements. All entries should be completed to the best of the supplier's ability.

This template can be downloaded from the AEC website at http://www.aecouncil.com.

Component Info:

#CDC-SUPPLIER	Supplier Name:	
#CDC-DEVICE NAME	Supplier Device Name:	
#CDC-DEVICE TYPE	Device Type:	
#CDC-PURPOSE	Document Purpose:	

Appendix 3: Plastic Package Opening for Wire Bond Testing

A3.1 Purpose

The purpose of this Appendix is to define a guideline for opening plastic packaged devices so that reliable wire pull or bond shear results will be obtained. This method is intended for use in opening plastic packaged devices to perform wire pull testing after temperature cycle testing or for bond shear testing.

A3.2 Materials and Equipment

A3.2.1 Etchants

Various chemical strippers and acids may be used to open the package dependent on your experience with these materials in removing plastic molding compounds. Red Fuming Nitric Acid has demonstrated that it can perform this function very well on novolac type epoxies, but other materials may be utilized if they have shown a low probability for damaging the bond pad material.

A3.2.2 Plasma Strippers

Various suitable plasma stripping equipment can be utilized to remove the plastic package material.

A3.3 Procedure

a. Using a suitable end mill type tool or dental drill, create a small impression just a little larger than the chip in the top of the plastic package. The depth of the impression should be as deep as practical without damaging the loop in the bond wires.

b. Using a suitable chemical etchant or plasma etcher, remove the plastic material from the surface of the die, exposing the die bond pad, the loop in the bond wire, and at least 75% of the bond wire length. Do not expose the wire bond at the lead frame (these bonds are frequently made to a silver plated area and many chemical etchants will quickly degrade this bond making wire pull testing impossible).

c. Using suitable magnification, inspect the bond pad areas on the chip to determine if the package removal process has significantly attacked the bond pad metallization. If a bond pad shows areas of missing metallization, the pad has been degraded and shall not be used for bond shear or wire pull testing. Bond pads that do not show attack can be used for wire bond testing.

Appendix 4: Minimum Requirements for Qualification Plans and Results

The following information is required as a minimum to identify a device that has met the requirements of AEC-Q100 (see Appendix Templates 4A and 4B). Submission of data in this format is optional. However, if these templates are not used, the supplier must ensure that each item on the template is adequately addressed. The templates can be downloaded from the AEC website at http://www.aecouncil.com.

A4.1 Plans

1. Part Identification: Customer P/N and supplier P/N.
2. Site or sites at which life testing will be conducted.
3. List of tests to be performed (e.g., JEDEC method, Q100 method, MIL-STD method) along with conditions. Include specific temperature(s), humidity, and bias to be used.
4. Sample size and number of lots required.
5. Time intervals for end-points (e.g., 0 hour, 500 hour, 1000 hour).
6. Targeted start and finish dates for all tests and end-points.
7. Supplier name and contact.
8. Submission date.
9. Material and functional details and test results of devices to be used as generic data for qualification. Include rationale for use of generic data.

A4.2 Results

All of above plus:

1. Date codes and lot codes of parts tested.
2. Process identification.
3. Fab and assembly locations.
4. Mask number or designation.
5. Number of failures and number of devices tested for each test.
6. Reports on failure analyses for all failures and proven corrective actions if applicable to be submitted with results.

Appendix Template 4A: AEC-Q100 Qualification Test Plan

Q100J QUALIFICATION TEST PLAN							
USER COMPANY:				DATE:			
USER P/N:				TRACKING NUMBER:			
USER SPEC #:				USER COMPONENT ENGINEER:			
SUPPLIER COMPANY:				SUPPLIER MANUFACTURING SITES:			
SUPPLIER P/N:				PPAP SUBMISSION DATE:			
SUPPLIER FAMILY TYPE:				REASON FOR QUALIFICATION:			
STRESS TEST	**ABV**	**TEST#**	**TEST METHOD**	**Test Conditions/S.S. per Lot/# Lots (identify temp, RH, & bias)**	**REQUIREMENTS**		**RESULTS Fails/S.S./# lots**
					S.S	**# LOTS**	
Preconditioning	PC	A1	JEDEC J-STD-020 JESD22-A113	Peak Reflow Temp. = Preconditioning used =	Min. MSL = 3		MSL =
Temperature Humidity Bias or HAST	THB / HAST	A2	JESD22-A101/A110		77	3	
Autoclave or Unbiased HAST or Temperature Humidity	AC / UHST / TH	A3	JESD22-A102/A118/A101		77	3	
Temperature Cycle	TC	A4	JESD22-A104		77	3	
Power Temperature Cycling	PTC	A5	JESD22-A105		45	1	
High Temperature Storage Life	HTSL	A6	JESD22-A103		45	1	
High Temperature Operating Life	HTOL	B1	JESD22-A108		77	3	
Early Life Failure Rate	ELFR	B2	AEC Q100-008		800	3	
NVM Endurance, Data Retention, & Operational Life	EDR	B3	AEC Q100-005		77	3	
Wire Bond Shear	WBS	C1	AEC Q100-001		5	1	
Wire Bond Pull Strength	WBP	C2	MIL-STD-883 - 2011		5	1	
Solderability	SD	C3	J-STD-002		15	1	
Physical Dimensions	PD	C4	JESD22-B100/B108		10	3	
Solder Ball Shear	SBS	C5	AEC Q100-010		10	3	
Lead Integrity	LI	C6	JESD22-B105		5	1	
Bump Shear	BST	C7	JESD22-B117	20 bumps/pillars from 5 devices	5	1	
Electromigration	EM	D1					
Time Dependent Dielectric Breakdown	TDDB	D2					
Hot Carrier Injection	HCI	D3					
Bias Temperature Instability	BTI	D4					
Stress Migration	SM	D5					
Pre- and Post-Stress Electrical Test	TEST	E1	Test to spec				
ESD - Human Body Model	HBM	E2	AEC Q100-002		See Test Method		
ESD - Charged Device Model	CDM	E3	AEC Q100-011		See Test Method		
Latch-Up	LU	E4	AEC Q100-004		3	1	
Electrical Distributions	ED	E5	AEC Q100-009		30	3	
Fault Grading	FG	E6	AEC-Q100-007				
Characterization	CHAR	E7	AEC Q003				
Electromagnetic Compatibility	EMC	E9	SAE J1752/3		1	1	
Short Circuit Characterization	SC	E10	AEC Q100-012		10	3	
Soft Error Rate	SER	E11	JESD89-1, -2, -3		3	1	
Lead Free	LF	E12	Q005				
Process Average Test	PAT	F1	AEC Q001				
Statistical Bin/Yield Analysis	SBA	F2	AEC Q002				
Hermetic Package Tests	MECH	G1-4	Series		15	1	
Package Drop	DROP	G5			5	1	
Lid Torque	LT	G6	MIL-STD-883 - 2024		5	1	
Die Shear Strength	DS	G7	MIL-STD-883 - 2019		5	1	
Internal Water Vapor	IWV	G8	MIL-STD-883 - 1018		5	1	
Supplier:				Approved by: (User Engineer)			

Appendix Template 4B: AEC-Q100 Generic Data

Objective:		*Package:*		*Qual Plan Ref #:*	
Device:		*Fab/Assy/Test:*		*Date Prepared:*	
Cust PN:		*Device Engr:*		*Prepared by:*	
Maskset:		*Product Engr:*		*Date Approved:*	
Die Size:		*Component Engr:*		*Approved by:*	

Test #	ABV	Q100 Test Conditions	End-Point Requirements	Sample Size/Lot	# of Lots	Total # Units	Part to be Qualified	Differences from Q100	Generic Family part A	Differences from Q100	Generic Family part B	Differences from Q100
A1	**PC**	JEDEC J-STD-020	TEST = ROOM	All surface mount parts prior to A2, A3, A4, A5								
A2	**THB / HAST**	JESD22-A101/A110	TEST = ROOM and HOT	77	3	231						
A3	**AC / UHST / TH**	JESD22-A102/A118/A101	TEST = ROOM	77	3	231						
A4	**TC**	JESD22-A104	TEST = HOT	77	3	231						
A5	**PTC**	JESD22-A105	TEST = ROOM and HOT	45	1							
A6	**HTSL**	JESD22-A103	TEST = ROOM and HOT	45	1							
B1	**HTOL**	JESD22-A108	TEST = ROOM, COLD, and HOT	77	3	231						
B2	**ELFR**	AEC Q100-008	TEST = ROOM and HOT	800	3	2400						
B3	**EDR**	AEC Q100-005	TEST = ROOM and HOT	77	3	231						
C1	**WBS**	AEC Q100-001	Cpk>1.67 and in SPC	An appropriate time period for each bonder to be used								
C2	**WBP**	MIL-STD-883 – 2011										
C3	**SD**	J-STD-002	per J-STD-002	15	1	15						
C4	**PD**	JESD22-B100/B108	Cpk > 1.67	10	3	30						
C5	**SBS**	AEC Q100-010	Two reflow cycles before SBS									
C6	**LI**	JESD22-B105	No lead breakage or finish cracks	10 leads from each of 5	1	5						
C7	**BST**	JESD22-B117		20 bumps/pillars from each of 5	1	5						
D1	**EM**											
D2	**TDDB**											
D3	**HCI**											
D4	**BTI**											
D5	**SM**											
E1	**TEST**		All parametric and functional tests	All units	-	All						
E2	**HBM**	AEC Q100-002	TEST = ROOM and HOT		1	Var.						
E3	**CDM**	AEC Q100-011	TEST = ROOM and HOT		1	Var.						
E4	**LU**	AEC Q100-004	TEST = ROOM and HOT	3	1	3						
E5	**ED**	AEC Q100-009	TEST = ROOM, HOT, and COLD	30	3	90						
E6	**FG**	AEC Q100-007										
E7	**CHAR**	AEC Q003										
E9	**EMC**	SAE J1752/3		1	1	1						
E10	**SC**	AEC Q100-012		10	3	30						
E11	**SER**	JESD89-1, -2, -3		3	1	3						
E12	**LF**	Q005										
F1	**PAT**	AEC Q001		All units	-	All						
F2	**SBA**	AEC Q002		All units	-	All						
G1	**MS**	JESD22-B104	TEST = ROOM	15	1	15						
G2	**VFV**	JESD22-B103	TEST = ROOM	15	1	15						
G3	**CA**	MIL-STD-883 – 2001	TEST = ROOM	15	1	15						
G4	**GFL**	MIL-STD-883 – 1014		15	1	15						
G5	**DROP**		TEST = ROOM	5	1	5						
G6	**LT**	MIL-STD-883 – 2024		5	1	5						
G7	**DS**	MIL-STD-883 – 2019		5	1	5						
G8	**IWV**	MIL-STD-883 - 1018		5	1	3						

Appendix Template 4B: AEC-Q100 Generic Data (continued)

Part Attributes	Part to be Qualified	Generic Family Part A	Generic Family Part B
User Part Number			
Supplier Part Number			
A1.1 Product			
Product Functionality (e.g., Op-Amp, Regulator, Microprocessor, Logic – HC/TTL)			
Operating Supply Voltage Range(s)			
Specified Operating Temperature Range			
Specified Operating Frequency Range			
[1] Analog Design Library Cells (e.g., active circuit elements, passive circuit elements)			
[1] Digital Design Library Cells (e.g., circuit blocks, IO modules, ESD cells)			
Memory IP (e.g., cell structure, building block)			
Memory Type(s) & Size(s)			
Design Rules for Active Circuits under Pads			
Other Functional Characteristics (as defined by supplier)			
A1.2 Fab Process			
Wafer Fab Technology (e.g., CMOS, NMOS, Bipolar)			
Circuit Element Feature Size (e.g., layout design rules, die shrinks, contacts, gates, isolations)			
Substrate (e.g., orientation, doping, epi, wafer size)			
Maximum Number of Masks (supplier must show justification for waiving this requirement)			
Lithographic Process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)			
Doping Process (e.g., diffusion vs. ion implantation)			
Gate Structure, Material & Process (e.g., polysilicon, metal, salicide, wet vs. dry etch)			
Polysilicon Material, Thickness Range, & Number of Levels			
Oxidation Process & Thickness Range (e.g., gate & field oxides)			
Interlevel Dielectric Material & Thickness Range			
Metallization Material, Thickness Range, & Maximum Number of Levels			
Passivation Process (e.g., passivation oxide opening), Material, & Thickness Range			
Die Backside Preparation Process & Metallization			
Wafer Fabrication Site			

Appendix Template 4B: AEC-Q100 Generic Data (continued)

Part Attributes	Part to be Qualified	Generic Family Part A	Generic Family Part B
A1.3 Assembly Process – Plastic, Ceramic, or Flip-Chip BGA			
Assembly Site			
Package Type (e.g., DIP, SOIC, QFP, PGA, PBGA, FC-BGA)			
Range of Paddle/Flag Size (maximum & minimum dimensions) Qualified for the Die Size/Aspect Ratio Under Consideration			
Worst Case Package (e.g., package warpage due to CTE mismatch)			
Substrate Base Material (e.g., PBGA, FC-BGA)			
Leadframe Base Material			
Die Header / Thermal Pad Material			
Leadframe Plating Material & Process (internal & external to the package)			
Die Attach Material			
Wire Bond Material & Diameter			
Wire Bond Method, Presence of Downbonds, & Process			
Plastic Mold Compound Material, Organic Substrate Material, or Ceramic Package Material			
Plastic Mold Compound Supplier/ID			
Solder Ball Metallization System (if applicable)			
Heatsink Type, Material, & Dimensions			
Underfill Material			
Redistribution Layer, UBM & Bump Material			
Die Preparation/Singulation			

Note 1: Design Library cells need to follow guidelines for temperature ranges, voltage ranges, speed, performance, and power dissipation as defined in Appendix 1.

Appendix 5: Part Design Criteria to Determine Need for EMC Testing

A5.1 EMC Part Design Criteria

Use the following criteria to determine if a part is a candidate for EMC testing:

a. Digital technology, LSI, products with oscillators or any technology that has the potential of producing radiated emissions capable of interfering with communication receiver devices. Examples include microprocessors, high speed digital IC's, FET's incorporating charge pumps, devices with watchdogs, and switch-mode regulator control and driver IC's.

b. All new, requalified, or existing IC's that have undergone revisions from previous versions that have the potential of producing radiated emissions capable of interfering with communication receiver devices.

A5.2 EMC Part Design Factors

Examples of factors that would be expected to affect radiated emissions:

- Clock drive (internal or external) I/O Drive
- Manufacturing process or material composition that reduces rise/fall times (e.g., lower E dielectric, lower p metallization)
- Minimum feature size (e.g., die shrink)
- Package or pinout configuration
- Leadframe material

Appendix 6: Part Design Criteria to Determine Need for SER Testing

A6.1 SER Part Design Criteria

Use the following criteria to determine if a part is a candidate for SER Testing:

a. The part use application will have a significant radiation exposure such as an aviation application or extended service life at higher altitudes.

b. SER testing is needed for devices with large numbers of SRAM or DRAM cells (≥ 1 Mbit). For example: Since the SER rates for a 130 nm technology are typically near 1000 FIT/MBIT, a device with only 1,000 SRAM cells will result in an SER contribution of ~1 FIT.

A6.2 SER Part Design Factors

Examples of factors that would be expected to affect SER results:

a. Technology shrink to small $L_{effective}$.

b. Package mold/encapsulate material.

c. Bump material making die to package connections for Flip Chip package applications.

d. Mitigating factors such as implementation of Error Correcting Code (ECC) and Soft Error Detection (SED).

A6.3 New SER Testing

Cases where new SER testing may be required:

a. Change in basic SRAM/DRAM transistor cell structure (e.g., L_{eff}, well depth and dopant concentration, isolation method).

Appendix 7: AEC-Q100 and the Use of Mission Profiles

A7.1 SCOPE

Successful completion of the test requirements in Table 2 allows the claim to be made that the part is AEC Q100 qualified. Additional testing may be agreed between suppliers and users depending on more demanding application environments. To address these more stringent conditions, application based Mission Profiles may be used for a reliability capability.

A mission profile is the collection of relevant environmental and functional loads that a component will be exposed to during its use lifetime.

A7.1.1 Purpose

This appendix provides information on an approach that can be used to assess the suitability of a component for a given application and its mission profile for unique requirements. The benefit of applying this approach is that, in the end, the reliability margin between the component (specification) space and the application (condition) space may be shown.

- Section A7.2 demonstrates the relation between AEC-Q100 stress conditions / durations and a typical example of a set of use life time and loading conditions.
- Section A7.3 describes the approach, supported by flow charts, which can be used for a reliability capability assessment starting from a mission profile description.

A7.1.2 References

- **JEDEC JEP122** Failure Mechanisms and Models for Semiconductor Devices

A7.2 BASE CONSIDERATIONS

A7.2.1 Use Lifetime and Mission Profile

The use lifetime assumptions drawn here are an example used for demonstration purpose only. Many typical mission profiles will differ in one or more characteristics from what is shown below.

- service lifetime in years
- engine on-time in hours
- engine off time { idle} in hours
- non-operating time in hours
- number of engine on-off cycles
- service mileage

The mission profile itself is generated by adding information on thermal, electrical, mechanical and any other forms of loading under use conditions to the above lifetime characteristics. Examples of these and how they relate to the test conditions in Table 2 are shown in Table A7.1.

A7.2.2 Relation to AEC-Q100 Stress Test Conditions and Durations

The example basic calculations in Table A7.1 for each of the major stress tests demonstrate how one can derive suitable test conditions for lifetime characteristics based on reasonable assumptions for the loading. Caution should always be taken on use of excessive test conditions beyond those in Table 2, because they may induce unrealistic failure mechanisms and/ or acceleration. Please note that the mission profile in Table A7.1 is for reference only, and should not be construed as absolute use conditions. It is highly recommended that a supplier consult with users in order to ensure the mission profile used is adequate for the intended applications.

A7.3 METHOD TO ASSESS A MISSION PROFILE

This section demonstrates how to perform a more detailed reliability capability assessment in cases where the application differs significantly from existing and proven situations:

- Application has a demanding loading profile
- Application has an extended service lifetime requirement
- Application has a more stringent failure rate target over lifetime

These considerations may result in extended test durations. In addition, there may be components manufactured in new technologies and/or containing new materials that are not yet qualified. In such cases, unknown failure mechanisms may occur with different times-to-failure which may require different test methods and/or conditions and/or durations.

For these cases, two flow charts are available to facilitate both the user and the supplier in a reliability capability assessment:

- Flow Chart 1 in Figure A7.1 describes the process at the supplier to assess whether a new component can be qualified by AEC-Q100.
- Flow Chart 2 in Figure A7.2 describes (1) the process at the user to assess whether a certain electronic component fulfills the requirements of the mission profile of a new Electronic Control Unit (ECU); and (2) the process at the supplier to assess whether an existing component qualified according to AEC-Q100 can be used in a new application.

For details on how to apply this method, please refer to SAE J1879, SAE J1211, and/or ZVEI Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications.

In summary, the flow charts result in the following three clear possible conclusions:

[A] AEC-Q100 test conditions do apply.

This part of the flow first provides the input for the assessment by generating the mission profile. A proper mission profile is the key for setting a meaningful test plan or performing any kind of reliability assessment.

Guidance for what should be taken into account is given in JESD94.

The decision for following the basic calculation flow should be based on the data which is available for the used technology. If the technology is mature, failure mechanisms are known and the models are well calibrated and mature, then the supplier shall do the basic calculation as described in the flow. The outcome is the proof that standard stress test conditions can be used.

Examples for cases when a basic calculation shall not be done but part B of the flow should be entered:

- Introduction of fundamental new materials/technologies (e.g., Si → SiC, Au wire → Cu wire, SiO_2 → high k dielectric)
- Fundamental new field of application with specific dominant failure mechanisms (e.g., long operating at moderate temperatures and high humidity)

[B] Mission Profile specific test conditions may apply.

There are two entry points to part B of the flow:

- First, the technology or materials are unknown to the supplier and/or might introduce unknown/uncharacterized failure mechanisms or the current acceleration models have not been verified. Then, ability to apply the basic calculation must be demonstrated or would be considered invalid.
- Second, the basic calculation indicates that the standard stress test conditions are not sufficient to validate the mission profile.

In both cases a mission profile specific qualification test plan is required. The stress test conditions shall be derived by taking the mission profile, the relevant failure mechanisms and acceleration models into account.

JESD94 provides guidance to the selection of the relevant failure mechanisms as well as to deriving or selecting the appropriate reliability and acceleration models.

[C] Robustness Validation may be applied with detailed alignment between user and supplier.

The flow so far targets still a qualification according to the mission profile on a product level. There might be limitation of doing so. Reasons for not performing a full qualification on a product level might be but are not limited to:

- Occurrence of failure mechanisms with high and low acceleration in the same product. The stress test condition to cover the low accelerated mechanism, might lead to wear out with respect to the high accelerated mechanism making it impossible to prove the lifetime requirement for both mechanisms on product level.
- Extremely long test times due to extraordinary mission profile durations.
- Insufficient observability of a failure mechanism on product level.

In that case the use of advanced reliability methods using generic data generated using test vehicles is recommended. This data is typically gathered during technology development and can be reused for reliability prediction. The Robustness Validation flow provides guidance how to generate and use this data.

In addition, not shown in the flow charts, the expected end of life failure rate may be an important criterion. Regarding failure rates, the following points should be considered:

- No fails in 231 devices (77 devices from 3 lots) are applied as pass criteria for the major environmental stress tests. This represents an LTPD (Lot Tolerance Percent Defective) = 1, meaning a maximum of 1% failures at 90% confidence level.
- This sample size is sufficient to identify intrinsic design, construction, and/or material issues affecting performance.
- This sample size is NOT sufficient or intended for process control or PPM evaluation. Manufacturing variation failures (low ppm issues) are achieved through proper process controls and/or screens such as described in AEC-Q001 and AEC-Q002.
- Three lots are used as a minimal assurance of some process variation between lots. A monitoring process has to be installed to keep process variations under control.
- Sample sizes are limited by part and test facility costs, qualification test duration and limitations in batch size per test.

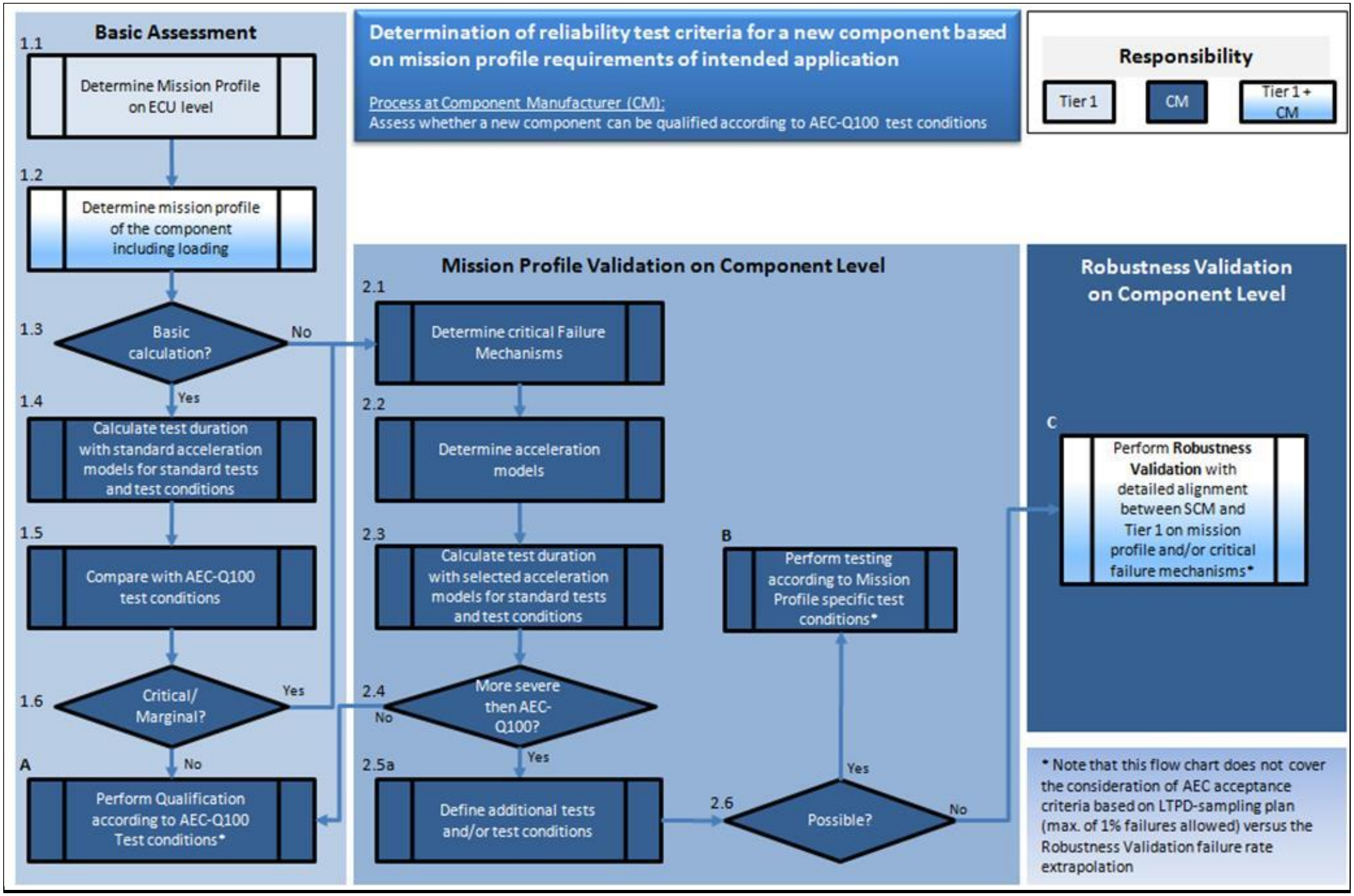


Figure A7.1: Flow Chart 1 – Reliability Test Criteria for New Component

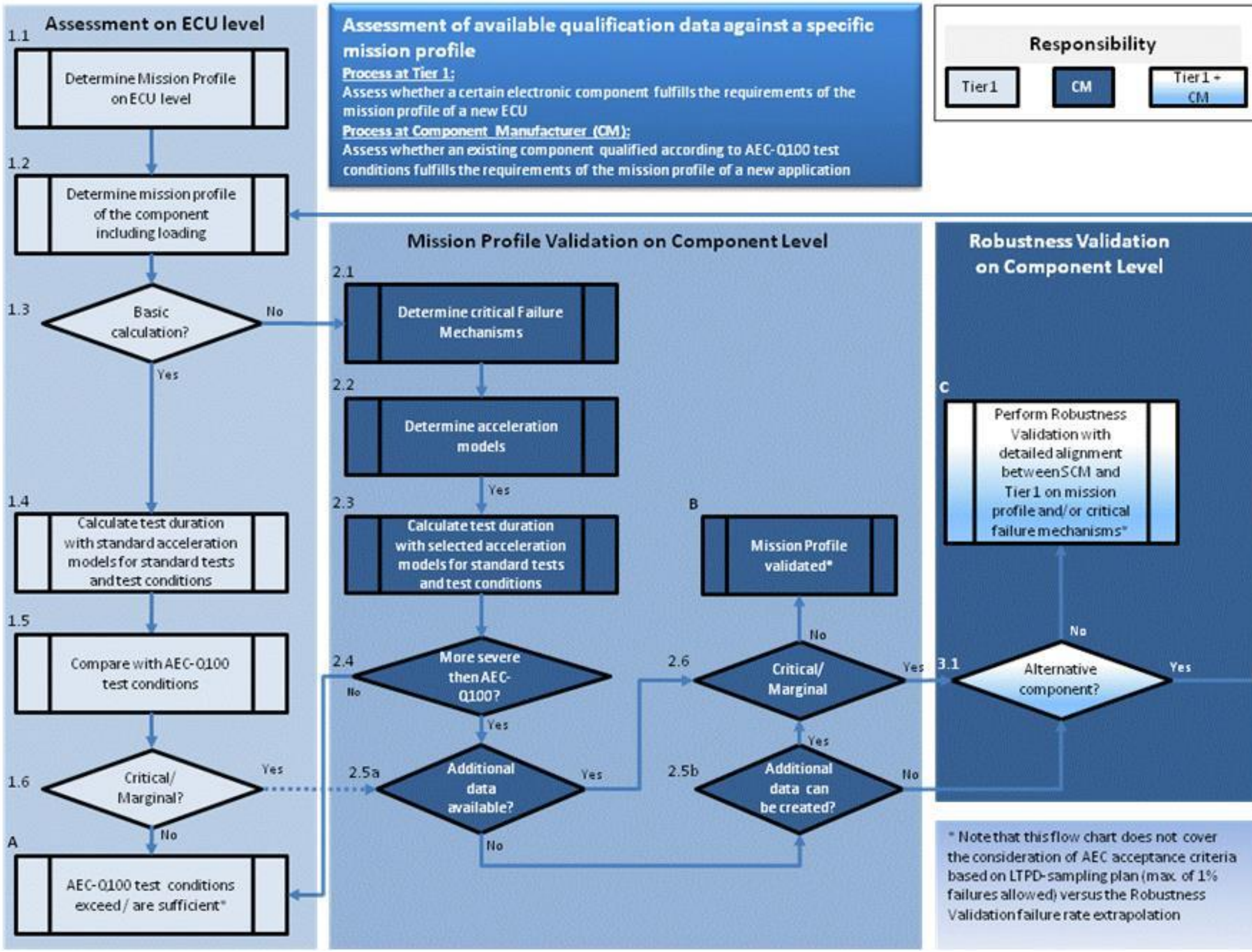


Figure A7.2: Flow Chart 2 – Assessment of Existing, Qualified Component

Table A7.1: Example Basic Calculations for AEC-Q100 Stress Test Conditions and Durations

Loading	Example Mission Profile Input	Stress Test	Stress Conditions	Acceleration Model (all temperatures in K, not in °C)	Model Parameters	Calculated Test Duration	Q100 Test Duration
Operation	t_u = 12,000 hr (average operating use time over 15 yr) T_u = 87°C (average junction temperature in use environment)	High Temperature Operating Life (HTOL)	T_t = 125°C (junction temperature in test environment)	Arrhenius $A_f = \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$ Also applicable for High Temperature Storage Life (HTSL) and NVM Endurance, Data Retention Bake, & Operational Life (EDR)	E_a = 0.7 eV (activation energy; 0.7 eV is a typical value, actual values depend on failure mechanism and range from -0.2 to 1.4 eV) k_B = 8.61733 x 10^{-5} eV/K (Boltzmann's Constant)	t_t = 1393 hr (test time) $t_t = \frac{t_u}{A_f}$	1000 hr
Thermo-mechanical	n_u = 54,750 cls (number of engine on/off cycles over 15 yr of use) ΔT_u =76°C (average thermal cycle temperature change in use environment)	Temperature Cycling (TC)	ΔT_t = 205°C (thermal cycle temperature change in test environment: -55°C to +150°C)	Coffin Manson $A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$ Also applicable for Power Temperature Cycle (PTC)	m = 4 (Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials)	n_t =1034 cls (number of cycles in test) $n_t = \frac{n_u}{A_f}$	1000 cls
Humidity (Option 1)	t_u = 131,400 hr (average on/off time over 15 yr of use) RH_u = 74% (average relative humidity in use environment) T_u = 32°C (average temperature in use environment: 9% @ 87°C - time on and 91% @ 27°C - time off)	Temperature Humidity Bias (THB)	RH_t = 85% (relative humidity in test environment) T_t = 85°C (ambient temperature in test environment)	Hallberg-Peck $A_f = \left(\frac{RH_t}{RH_u}\right)^p \bullet \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$ Also applicable for Highly Accelerated Steam Test (HAST) and Unbiased Humidity Steam Test (UHST). See Notes.	p = 3 (Peck exponent, 3 is to be used for bond pad corrosion) E_a = 0.8 eV (activation energy; 0.8 eV is to be used for bond pad corrosion) k_B = 8.61733 x 10^{-5} eV/K (Boltzmann's Constant)	T_t = 960 hr $t_t = \frac{t_u}{A_f}$	1000 hr

Table A7.1: Example Basic Calculations for AEC-Q100 Stress Test Conditions and Durations (continued)

Loading	Example Mission Profile Input	Stress Test	Stress Conditions	Acceleration Model (all temperatures in K, not in °C)	Model Parameters	Calculated Test Duration	Q100 Test Duration
Humidity (Option 2)	t_u = 131,400 hr (average on/off time over 15 yr of use) RH_u = 74% (average relative humidity in use environment) T_u = 32°C (average temperature in use environment: 9% @ 87°C - time on and 91% @ 27°C - time off)	Highly Accelerated Steam Test (HAST)	RH_t = 85% (relative humidity in test environment) T_t = 130°C (ambient temperature in test environment)	Hallberg-Peck $A_f = \left(\frac{RH_t}{RH_u}\right)^p \bullet \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$ Also applicable for Temperature Humidity Bias (THB) and Unbiased Humidity Steam Test (UHST). See Notes.	p = 3 (Peck exponent, 3 is to be used for bond pad corrosion) E_a = 0.8 eV (activation energy; 0.8 eV is to be used for bond pad corrosion) k_B = 8.61733 x 10^{-5} eV/K (Boltzmann's Constant)	T_t = 53 hr $t_t = \frac{t_u}{A_f}$	96 hr

Notes:

- Autoclave (121°C/100%RH) is a highly accelerated test using a saturated moisture condition that will tend to uncover failure mechanisms not seen in normal use conditions. For this reason, autoclave is not a test whose test conditions can be derived through models and assumptions. The current test conditions were selected decades ago and the test has been used as part of a standard qualification ever since.

- Most Pressure Pot testing is performed with an Al Pressure Pot. Air purging is done at 100°C boiling water, and with both steam and liquid escaping from the vent. The chamber walls are not independently heated at all. Control of the chamber wall temperature; air purging procedure, during ramp-up; ramp-down temperature and pressure and overall temperature and pressure are key. In addition, when the test is ended the heater is turned off and the vent is opened. It takes about 3 minutes to fully vent the pot. A significant concern is that venting before the pot chamber drops to 100°C, can cause a pressure differential from the >100°C residual hot device and cause any water trapped in device void to create a pop-corning type of delamination.

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release.
A	May 19, 1995	Added copyright statement. Revised sections 2.3, 2.4.1, 2.4.4, 2.4.5, 2.8, 3.2 and 4.2, Tables 2, 3, 4 and Appendix 1, 2. Added Appendix 3.
B	Sept. 6, 1996	Revised sections 1.1, 1.2.3, 2.3, 3.1, and 3.2.1, Tables 2, 3, and 4, and Appendix 2.
C	Oct. 8, 1998	Revised sections 1.1, 1.1.3, 1.2.2, 2.2, 2.3, 2.4.2, 2.4.5, 2.6, 3.1, 3.2.1, 3.2.3, 2.3.4, 4.1, and 4.2, Tables 3 and 4, Appendix 2, and Appendix 3. Added section 1.1.1, Figures 1, 2, and 3, and Test Methods Q100-008 and -009. Deleted sections 2.7 and 2.8.
D	Aug. 25, 2000	Revised sections 1.1 and 2.3, Figures 2, 3, and 4, Tables 2, 3, and 4, Appendix 1, and Appendix 2. Added section 2.3.2, Test Methods Q100-010 and -011, and Figure 1.
E	Jan. 31, 2001	Revised Figure 4.
F	July 18, 2003	Complete Revision.
G	May 14, 2007	Complete Revision. Revised document title to reflect that the stress test qualification requirements are failure mechanism based. Revised sections 1, 1.1, 1.2.1, 1.2.2, 1.2.3, 2.3.1, 2.4.4, 2.5, 3.2, 3.2.3, 4.2, and 4.3, Figure 2, Tables 2 and 3, Appendix 2, Appendix 4A, and Appendix 4B. Added sections 2.1.1, 3.1.1, Table 2 and 3 entries (test #D4, D5, E10, and E11), Appendix 6, and Test Method Q100-012. Deleted Table 2A.
H	Sept. 11, 2014	Complete Revision. Revised sections 1.2.1, 1.3.1, 1.3.3, 2.2, 2.3.1, 2.3.3, 2.4.1, 2.4.5, 2.5, and 3.2.3, Figure 2, Tables 1 and 2, Appendix 1, Appendix 4A, Appendix 4B, and Revision History. Added Revision Summary, sections 1.2.4, 1.3.2, 1.3.4, 1.3.5, and 3.3, Table 2 and 3 entry (test #E12), Table 2 Legend (Note L), Tables A1.1 and A1.2, Appendix 7, Figures A7.1 and A7.2, and Table A7.1. Deleted section 3.1.1, Table 2 and 3 entries (test #E2 and E8).
I	unreleased	see Rev. J
J	Aug. 11, 2023	Complete Revision. Revised document title to clearly state the automotive focus. Revised sections 1.2.1, 1.2.3, 1.2.4, 1.3.1, 3.3, 4.3, Table 2, Table 3, Figure 3 Appendix 1, Appendix 2, Appendix Templates 4A, 4B, Appendix 7 New sections 1.3.6, 2.3, 3.6, Figure
J1	March 24, 2026	Appendix 2 (NOTE: underlined areas showing differences include J and J1)